

FIG. 1

100 →

FIG. 1

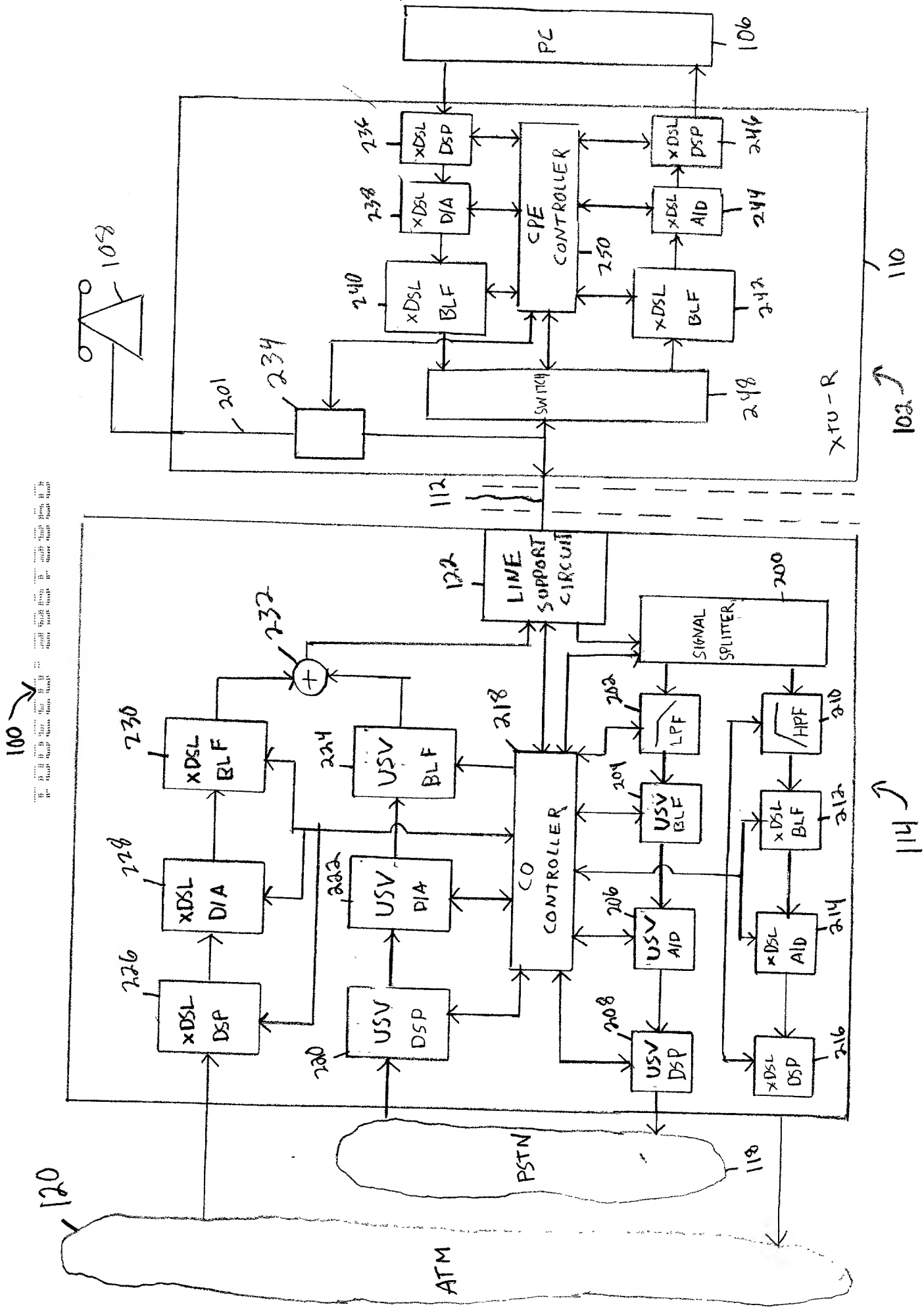


FIG. 2



FIG. 4 is a block diagram of a system 114 for processing signals. The system 114 includes a Controller 218, a USV DSP 220, a USV D/A 222, a USV BLF 224, an xDSL DSP 226, an xDSL D/A 228, an xDSL BLF 230, a USV Battery Feed/Line Interface Circuit/Transformer 402, an xDSL Line Driver and Transformer 404, a USV DSP 208, a USV A/D 206, a USV BLF 204, an xDSL DSP 216, an xDSL A/D 214, an xDSL BLF 212, a Low Pass Filter (LPF) 202, and a High Pass Filter (HPF) 210. The system 114 is configured to process signals between a USV and an xDSL line.

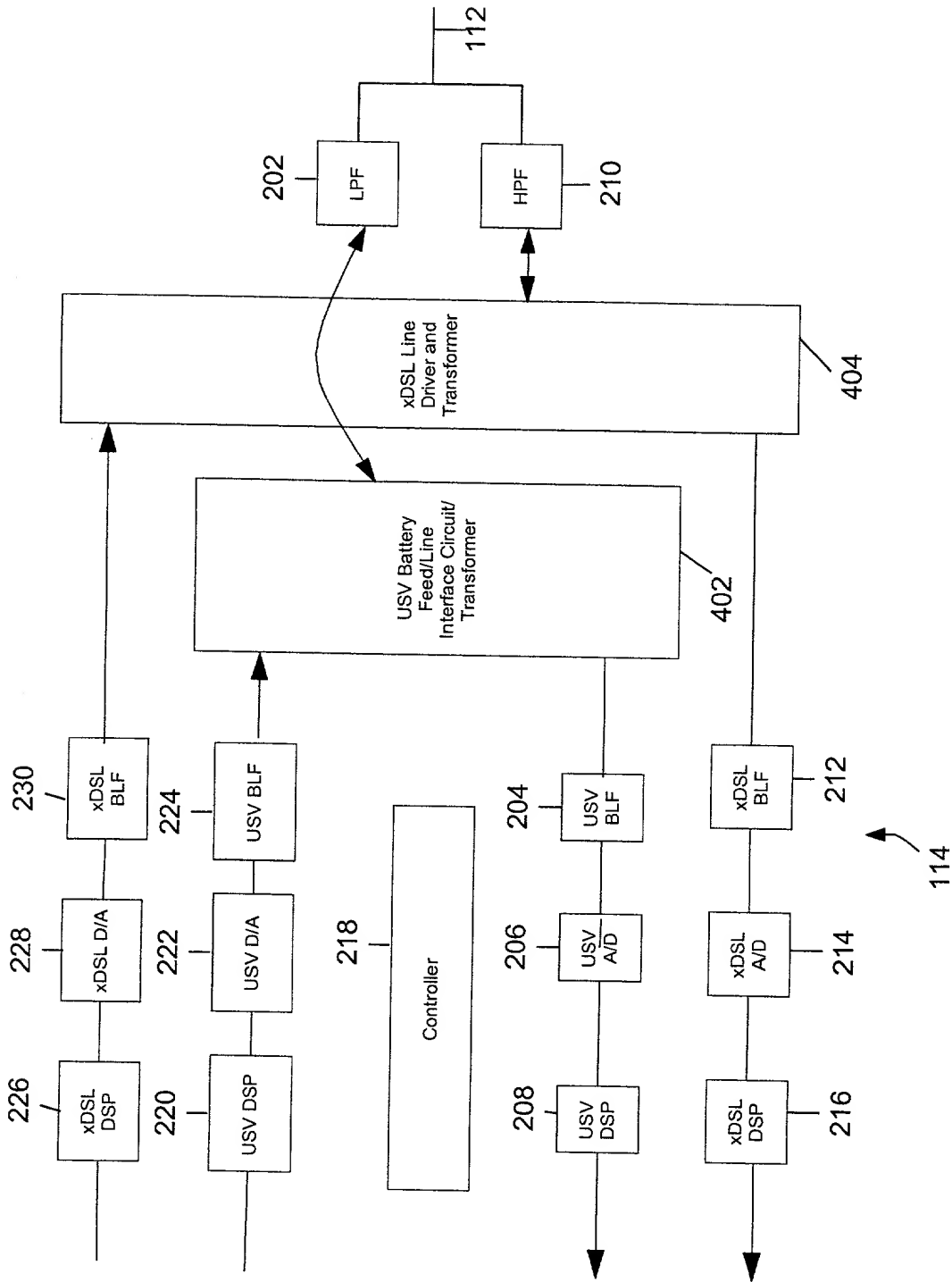


FIG. 4

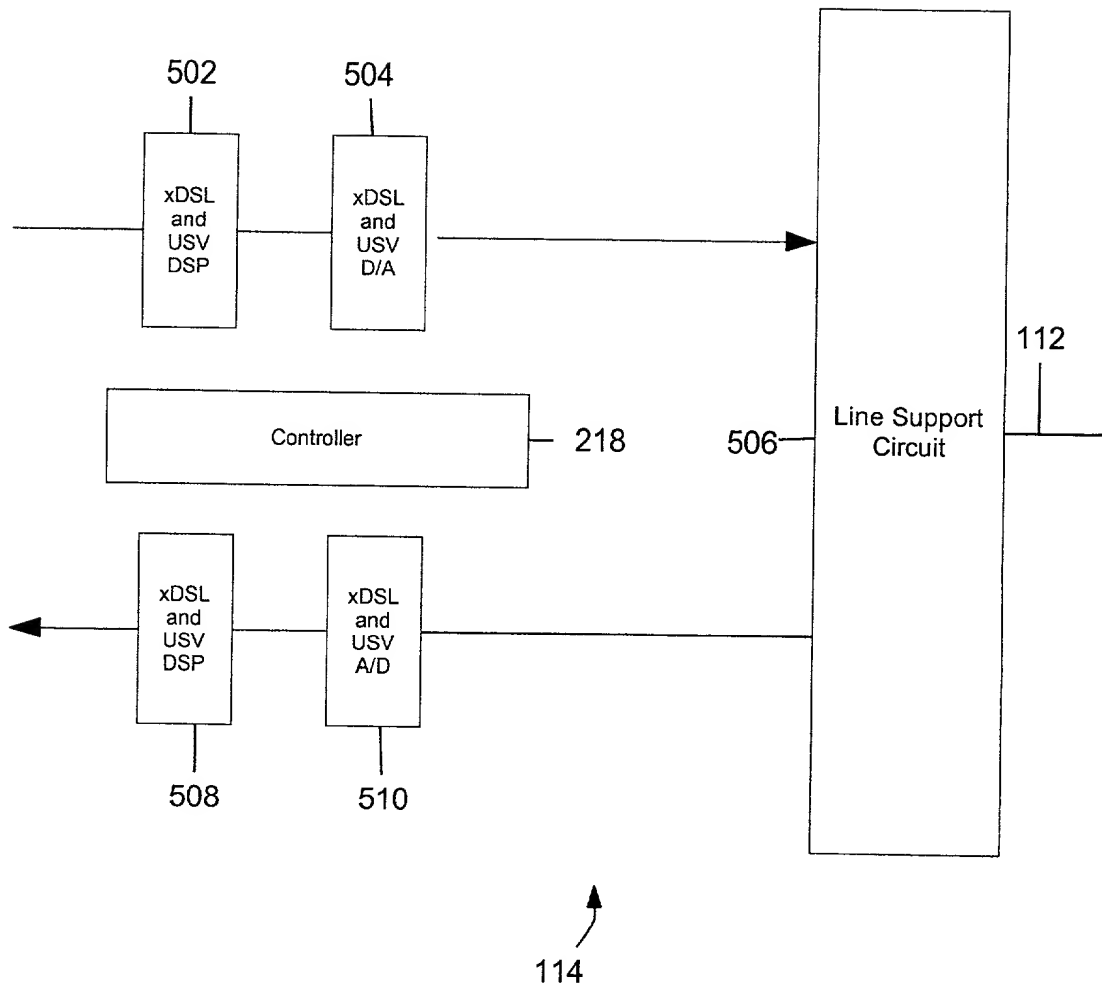


FIG. 5